

MODELING MICROPROCESSOR PERFORMANCE

Balocho, Guruswami
Kannath, Floze

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Modeling Microprocessor Performance

Richard Bailey



Modeling Microprocessor Performance:

Modeling Microprocessor Performance Bibiche Geuskens, Kenneth Rose, 2012-12-06 Modeling Microprocessor Performance focuses on the development of a design and evaluation tool named RIPE Rensselaer Interconnect Performance Estimator This tool analyzes the impact on wireability clock frequency power dissipation and the reliability of single chip CMOS microprocessors as a function of interconnect device circuit design and architectural parameters It can accurately predict the overall performance of existing microprocessor systems For the three major microprocessor architectures DEC PowerPC and Intel the results have shown agreement within 10% on key parameters The models cover a broad range of issues that relate to the implementation and performance of single chip CMOS microprocessors The book contains a detailed discussion of the various models and the underlying assumptions based on actual design practices As such RIPE and its models provide an insightful tool into single chip microprocessor design and its performance aspects At the same time it provides design and process engineers with the capability to model evaluate compare and optimize single chip microprocessor systems using advanced technology and design techniques at an early design stage without costly and time consuming implementation RIPE and its models demonstrate the factors which must be considered when estimating tradeoffs in device and interconnect technology and architecture design on microprocessor performance

Analytical Modeling of Modern Microprocessor Performance, 2006 As the number of transistors integrated on a chip continues to increase a growing challenge is accurately modeling performance in the early stages of processor design Analytical modeling is an alternative to detailed simulation with the potential to shorten the development cycle and provide additional insight This thesis proposes hybrid analytical models to predict the impact of pending cache hits hardware prefetching and realistic miss status holding register MSHR resources on superscalar performance We propose techniques to model the non negligible influences of pending hits and the fine grained selection of instruction profile window blocks on the accuracy of hybrid analytical models We also present techniques to estimate the performance impact of data prefetching by modeling the timeliness of prefetches and to account for a limited number of MSHRs by restricting the size of profile window blocks As with earlier hybrid analytical models our approach is roughly two orders of magnitude faster than detailed simulations Overall our techniques reduce the error of our baseline from 39.7% to 10.3% when the number of MSHRs is unlimited When modeling a processor with data prefetching a limited number of MSHRs or both our techniques result in an average error of 13.8%, 9.5% and 17.8% respectively Moreover this thesis proposes analytical models for predicting the cache contention and throughput of heavily fine grained multithreaded architectures such as Sun Microsystems Niagara We first propose a novel probabilistic model using statistics characterizing individual threads run in isolation as inputs to accurately predict the number of extra cache misses due to cache contention among a large number of threads We then present a Markov chain model for analytically estimating the throughput of multicore fine grained multithreaded architectures Combined the two

models accurately predict system throughput obtained from a detailed simulator with an average Single and Multi-CPU Performance Modeling for Embedded Systems Trevor Conrad Meyerowitz,2008 **Processor Modeling and Evaluation Techniques for Early Design Stage Performance Comparison** John-David Wellman,1996 The Anatomy of a High-Performance Microprocessor Bruce Shriver,Bennett Smith,1998-06-18 This work describes in detail the microarchitecture of a high performance microprocessor giving an integrated treatment of platform and systems issues relating to the design and implementation of microprocessor based systems This book is a reference for individuals building systems using microprocessors and readers looking for significant insights into fundamental design guidelines that transcend the design implementation and use of a specific microprocessor Practitioners academics and technical and product managers alike will benefit from this detailed overview of microprocessors platforms and systems for years in the future

Evaluation of a Processor's Performance by Modeling Michael Jay Newman,1976 *Performance and Fault Modeling with VHDL* Joel Mark Schoen,1992 Describes how VHDL can be used across the system design process from specification to the development of maintenance strategies The contributors provide advanced techniques and detail how these can be adapted to improve the system development process reducing time and cost **High Performance Computing** ,1999 **Modelling Techniques and Tools for Performance Analysis** D. Potier,1985 *Modeling and Simulation* ,1990 Computer Systems Performance Modeling Charles H. Sauer,K. Mani Chandy,1981 *High Performance Systems* ,1990 2001 International Workshop on System-Level Interconnect Prediction ,2001 The SLIP workshop is a forum for the exchange of ideas at the interface between interconnect technology and physical design This year in recognition of the highly diverse backgrounds and motivations of the attendees SLIP 2001 has been organized around three mini tutorials a review of wire distribution models a look under the hood of a variety of system level interconnect modeling programs and back end of line yield modeling These tutorials set the scene for the paper sessions that follow Forward **Cockpit Displays** ,1995 **Building an Advanced Climate Model** ,1990 *Electrical Performance of Electronic Packaging* ,2004 *Innovative Architecture for Future Generation High-performance Processors and Systems* Alex Veidenbaum,Kazuki Joe,2003 This edited volume presents a collection of papers from the 2003 International Workshop on Innovative Architecture for Future Generation High Performance Processors and Systems IWIA 03 It looks at a number of important issues in the areas of computer architecture compilers and applications and this year s special topic is embedded processor design with focus on memory hierarchy High performance computing is extensively discussed as well One of the workshop highlights is the presentation and discussion of the Earth Simulator supercomputer being constructed in Japan to study global change phenomena **Index to IEEE Publications** Institute of Electrical and Electronics Engineers,1989 Issues for 1973 cover the entire IEEE technical literature **Proceedings - Comcon** ,1982 *Modeling on Micros and Workstations* Thomas A. Rathburn,1991

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