

Networks-on-Chip

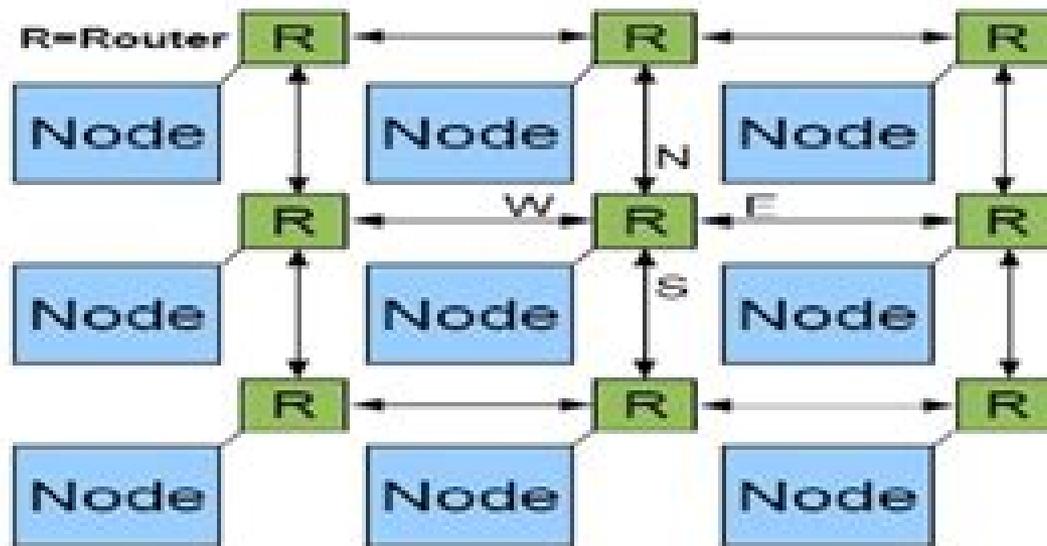


Figure 1. A typical NoC mesh.

Networks On Chip

Axel Jantsch, Hannu Tenhunen



Networks On Chip:

Networks on Chip Axel Jantsch, Hannu Tenhunen, 2007-05-08 As the number of processor cores and IP blocks integrated on a single chip is steadily growing a systematic approach to design the communication infrastructure becomes necessary Different variants of packed switched on chip networks have been proposed by several groups during the past two years This book summarizes the state of the art of these efforts and discusses the major issues from the physical integration to architecture to operating systems and application interfaces It also provides a guideline and vision about the direction this field is moving to Moreover the book outlines the consequences of adopting design platforms based on packet switched network The consequences may in fact be far reaching because many of the topics of distributed systems distributed real time systems fault tolerant systems parallel computer architecture parallel programming as well as traditional system on chip issues will appear relevant but within the constraints of a single chip VLSI implementation [Networks-on-Chips](#) Fayez Gebali, Haytham Elmiligi, Mohamed Watheq El-Kharashi, 2011-06-03 The implementation of networks on chip NoC technology in VLSI integration presents a variety of unique challenges To deal with specific design solutions and research hurdles related to intra chip data exchange engineers are challenged to invoke a wide range of disciplines and specializations while maintaining a focused approach Leading Researchers Present Cutting Edge Designs Tools Networks on Chips Theory and Practice facilitates this process detailing the NoC paradigm and its benefits in separating IP design and functionality from chip communication requirements and interfacing It starts with an analysis of 3 D NoC architectures and progresses to a discussion of NoC resource allocation processor traffic modeling and formal verification with an examination of protocols at different layers of abstraction An exploration of design methodologies CAD tool development and system testing as well as communication protocol the text highlights important emerging research issues such as Resource Allocation for Quality of Service QoS on chip communication Testing verification and network design methodologies Architectures for interconnection real time monitoring and security requirements Networks on Chip Protocols Presents a flexible MPSoC platform to easily implement multimedia applications and evaluate future video encoding standards This useful guide tackles power and energy issues in NoC based designs addressing the power constraints that currently limit the embedding of more processing elements on a single chip It covers traffic modeling and discusses the details of traffic generators Using unique case studies and examples it covers theoretical and practical issues guiding readers through every phase of system design **On-Chip Networks, Second Edition** Natalie Enright Jerger, Tushar Krishna, Li-Shiuan Peh, 2022-05-31 This book targets engineers and researchers familiar with basic computer architecture concepts who are interested in learning about on chip networks This work is designed to be a short synthesis of the most critical concepts in on chip network design It is a resource for both understanding on chip network basics and for providing an overview of state of the art research in on chip networks We believe that an overview that teaches both fundamental concepts and highlights state of the art designs will be of great value

to both graduate students and industry engineers While not an exhaustive text we hope to illuminate fundamental concepts for the reader as well as identify trends and gaps in on chip network research With the rapid advances in this field we felt it was timely to update and review the state of the art in this second edition We introduce two new chapters at the end of the book We have updated the latest research of the past years throughout the book and also expanded our coverage of fundamental concepts to include several research ideas that have now made their way into products and in our opinion should be textbook concepts that all on chip network practitioners should know For example these fundamental concepts include message passing multicast routing and bubble flow control schemes

Routing Algorithms in Networks-on-Chip

Maurizio Palesi, Masoud Daneshtalab, 2013-10-22 This book provides a single source reference to routing algorithms for Networks on Chip NoCs as well as in depth discussions of advanced solutions applied to current and next generation many core NoC based Systems on Chip SoCs After a basic introduction to the NoC design paradigm and architectures routing algorithms for NoC architectures are presented and discussed at all abstraction levels from the algorithmic level to actual implementation Coverage emphasizes the role played by the routing algorithm and is organized around key problems affecting current and next generation many core SoCs A selection of routing algorithms is included specifically designed to address key issues faced by designers in the ultra deep sub micron UDSM era including performance improvement power energy and thermal issues fault tolerance and reliability

Bio-Inspired Fault-Tolerant Algorithms for

Network-on-Chip Muhammad Athar Javed Sethi, 2020-03-17 Network on Chip NoC addresses the communication requirement of different nodes on System on Chip The bio inspired algorithms improve the bandwidth utilization maximize the throughput and reduce the end to end latency and inter flit arrival time This book exclusively presents in depth information regarding bio inspired algorithms solving real world problems focussing on fault tolerant algorithms inspired by the biological brain and implemented on NoC It further documents the bio inspired algorithms in general and more specifically in the design of NoC It gives an exhaustive review and analysis of the NoC architectures developed during the last decade according to various parameters Key Features Covers bio inspired solutions pertaining to Network on Chip NoC design solving real world examples Includes bio inspired NoC fault tolerant algorithms with detail coding examples Lists fault tolerant algorithms with detailed examples Reviews basic concepts of NoC Discusses NoC architectures developed to date

Networks on Chips Giovanni De Micheli, Luca Benini, 2006-08-30 The design of today s semiconductor chips for various applications such as telecommunications poses various challenges due to the complexity of these systems These highly complex systems on chips demand new approaches to connect and manage the communication between on chip processing and storage components and networks on chips NoCs provide a powerful solution This book is the first to provide a unified overview of NoC technology It includes in depth analysis of all the on chip communication challenges from physical wiring implementation up to software architecture and a complete classification of their various Network on Chip approaches and

solutions Leading edge research from world renowned experts in academia and industry with state of the art technology implementations trends An integrated presentation not currently available in any other book A thorough introduction to current design methodologies and chips designed with NoCs

Reliability, Availability and Serviceability of Networks-on-Chip Érika Cota,Alexandre de Moraes Amory,Marcelo Soares Lubaszewski,2011-09-23 This book presents an overview of the issues related to the test diagnosis and fault tolerance of Network on Chip based systems It is the first book dedicated to the quality aspects of NoC based systems and will serve as an invaluable reference to the problems challenges solutions and trade offs related to designing and implementing state of the art on chip communication architectures

Designing 2D and 3D Network-on-Chip Architectures Konstantinos Tatas,Kostas Siozios,Dimitrios Soudris,Axel Jantsch,2013-10-08 This book covers key concepts in the design of 2D and 3D Network on Chip interconnect It highlights design challenges and discusses fundamentals of NoC technology including architectures algorithms and tools Coverage focuses on topology exploration for both 2D and 3D NoCs routing algorithms NoC router design NoC based system integration verification and testing and NoC reliability Case studies are used to illuminate new design methodologies

Designing Reliable and Efficient Networks on Chips Srinivasan Murali,2009-05-26 Developing NoC based interconnect tailored to a particular application domain satisfying the application performance constraints with minimum power area overhead is a major challenge With technology scaling as the geometries of on chip devices reach the physical limits of operation another important design challenge for NoCs will be to provide dynamic run time support against permanent and intermittent faults that can occur in the system The purpose of Designing Reliable and Efficient Networks on Chips is to provide state of the art methods to solve some of the most important and time intensive problems encountered during NoC design

Network-on-Chip Santanu Kundu,Santanu Chattopadhyay,2018-09-03 Addresses the Challenges Associated with System on Chip Integration Network on Chip The Next Generation of System on Chip Integration examines the current issues restricting chip on chip communication efficiency and explores Network on chip NoC a promising alternative that equips designers with the capability to produce a scalable reusable and high performance communication backbone by allowing for the integration of a large number of cores on a single system on chip SoC This book provides a basic overview of topics associated with NoC based design communication infrastructure design communication methodology evaluation framework and mapping of applications onto NoC It details the design and evaluation of different proposed NoC structures low power techniques signal integrity and reliability issues application mapping testing and future trends Utilizing examples of chips that have been implemented in industry and academia this text presents the full architectural design of components verified through implementation in industrial CAD tools It describes NoC research and developments incorporates theoretical proofs strengthening the analysis procedures and includes algorithms used in NoC design and synthesis In addition it considers other upcoming NoC issues such as low power NoC design signal integrity issues NoC testing reconfiguration synthesis and 3

D NoC design This text comprises 12 chapters and covers The evolution of NoC from SoC its research and developmental challenges NoC protocols elaborating flow control available network topologies routing mechanisms fault tolerance quality of service support and the design of network interfaces The router design strategies followed in NoCs The evaluation mechanism of NoC architectures The application mapping strategies followed in NoCs Low power design techniques specifically followed in NoCs The signal integrity and reliability issues of NoC The details of NoC testing strategies reported so far The problem of synthesizing application specific NoCs Reconfigurable NoC design issues Direction of future research and development in the field of NoC Network on Chip The Next Generation of System on Chip Integration covers the basic topics technology and future trends relevant to NoC based design and can be used by engineers students and researchers and other industry professionals interested in computer architecture embedded systems and parallel distributed systems

Low Power Networks-on-Chip Cristina Silvano,Marcello Lajolo,Gianluca Palermo,2010-09-24 In recent years both Networks on Chip as an architectural solution for high speed interconnect and power consumption as a key design constraint have continued to gain interest in the design and research communities This book offers a single source reference to some of the most important design techniques proposed in the context of low power design for networks on chip architectures

Reconfigurable Networks-on-Chip Sao-Jie Chen,Ying-Cherng Lan,Wen-Chung Tsai,Yu-Hen Hu,2011-12-16 This book provides a comprehensive survey of recent progress in the design and implementation of Networks on Chip It addresses a wide spectrum of on chip communication problems ranging from physical network to application layers Specific topics that are explored in detail include packet routing resource arbitration error control correction application mapping and communication scheduling Additionally a novel bi directional communication channel NoC BiNoC architecture is described with detailed explanation Written for practicing engineers in need of practical knowledge about the design and implementation of networks on chip Includes tutorial like details to introduce readers to a diverse range of NoC designs as well as in depth analysis for designers with NoC experience to explore advanced issues Describes a variety of on chip communication architectures including a novel bi directional communication channel NoC From the Foreword Overall this book shows important advances over the state of the art that will affect future system design as well as R D in tools and methods for NoC design It represents an important reference point for both designers and electronic design automation researchers and developers Giovanni De Micheli Packet Switched Scalable On-chip Interconnection Architecture Design and Implementation for Networks-on-chip Daewook Kim,2006 Source-Synchronous Networks-On-Chip Ayan Mandal,Sunil P. Khatri,Rabi Mahapatra,2013-11-19 This book describes novel methods for network on chip NoC design using source synchronous high speed resonant clocks The authors discuss NoCs from the bottom up providing circuit level details before providing architectural simulations As a result readers will get a complete picture of how a NoC can be designed and optimized Using the methods described in this book readers are enabled to design NoCs that are 5X better than existing

approaches in terms of latency and throughput and can also sustain a significantly greater amount of traffic

On-chip Communication Kanishka Lahiri,2003 IEEE/ACM/IFIP International Conference on Hardware/Software Codesign & System Synthesis ,2005 *Networks-on-Chip* Sheng Ma,Libo Huang,Mingche Lai,Wei Shi,2014-12-04 *Networks on Chip From Implementations to Programming Paradigms* provides a thorough and bottom up exploration of the whole NoC design space in a coherent and uniform fashion from low level router buffer and topology implementations to routing and flow control schemes to co optimizations of NoC and high level programming paradigms This textbook is intended for an advanced course on computer architecture suitable for graduate students or senior undergrads who want to specialize in the area of computer architecture and Networks on Chip It is also intended for practitioners in the industry in the area of microprocessor design especially the many core processor design with a network on chip Graduates can learn many practical and theoretical lessons from this course and also can be motivated to delve further into the ideas and designs proposed in this book Industrial engineers can refer to this book to make practical tradeoffs as well Graduates and engineers who focus on off chip network design can also refer to this book to achieve deadlock free routing algorithm designs Provides thorough and insightful exploration of NoC design space Description from low level logic implementations to co optimizations of high level program paradigms and NoCs The coherent and uniform format offers readers a clear quick and efficient exploration of NoC design space Covers many novel and exciting research ideas which encourage researchers to further delve into these topics Presents both engineering and theoretical contributions The detailed description of the router buffer and topology implementations comparisons and analysis are of high engineering value *Proceedings* ,2007 *Proceedings of Technical Papers* ,2005

The Handbook of Computer Networks, Distributed Networks, Network Planning, Control, Management, and New Trends and Applications Hossein Bidgoli,2008 The Handbook of Computer Networks is the third set of reference books from leading author and Professor of Management Information Systems at California State University Bakersfield Hossein Bidgoli The Handbook of Computer Networks is designed to arm researchers practitioners students and managers with in depth understanding of this important and fast growing field in its broadest scope and in an applied and functional framework Each volume incorporates state of the art core information and networking topics practical applications and coverage of the emerging issues in the computer networking and data communications fields

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Networks On Chip Introduction

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