
Parallel Algorithms and Architectures for DSP Applications

**edited by
Magdy A. Bayoumi**



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Parallel Algorithms And Architectures For Dsp Applications

Lori Ellen Lucke



Parallel Algorithms And Architectures For Dsp Applications:

Parallel Algorithms and Architectures for DSP Applications Magdy A. Bayoumi, 2012-12-06 Over the past few years the demand for high speed Digital Signal Processing DSP has increased dramatically New applications in real time image processing satellite communications radar signal processing pattern recognition and real time signal detection and estimation require major improvements at several levels algorithmic architectural and implementation These performance requirements can be achieved by employing parallel processing at all levels Very Large Scale Integration VLSI technology supports and provides a good avenue for parallelism Parallelism offers efficient solutions to several problems which can arise in VLSI DSP architectures such as 1 Intermediate data communication and routing several DSP algorithms such as FFT involve excessive data routing and reordering Parallelism is an efficient mechanism to minimize the silicon cost and speed up the processing time of the intermediate middle stages 2 Complex DSP applications the required computation is almost doubled Parallelism will allow two similar channels processing at the same time The communication between the two channels has to be minimized 3 Application specific systems this emerging approach should achieve real time performance in a cost effective way 4 Testability and fault tolerance reliability has become a required feature in most of DSP systems To achieve such property the involved time overhead is significant Parallelism may be the solution to maintain acceptable speed performance

Software for Parallel Computation Janusz S. Kowalik, Lucio Grandinetti, 2012-12-06 This volume contains papers presented at the NATO sponsored Advanced Research Workshop on Software for Parallel Computation held at the University of Calabria Cosenza Italy from June 22 to June 26 1992 The purpose of the workshop was to evaluate the current state of the art of the software for parallel computation identify the main factors inhibiting practical applications of parallel computers and suggest possible remedies In particular it focused on parallel software programming tools and practical experience of using parallel computers for solving demanding problems Critical issues relative to the practical use of parallel computing included portability reusability and debugging parallelization of sequential programs construction of parallel algorithms and performance of parallel programs and systems In addition to NATO the principal sponsor the following organizations provided a generous support for the workshop CERFACS France C I R A Italy C N R Italy University of Calabria Italy ALENIA Italy The Boeing Company U S A CISE Italy ENEL D S R Italy Alliant Computer Systems Bull RN Sud Italy Convex Computer Digital Equipment Corporation Hewlett Packard Meiko Scientific U K PARSYTEC Computer Germany TELMAT Informatique France Thinking Machines Corporation

Annual ACM Symposium on Parallel Algorithms and Architectures, 2002

VLSI Design Methodologies for Digital Signal Processing Architectures Magdy A.

Bayoumi, 2012-12-06 Designing VLSI systems represents a challenging task It is a transposition among different specifications corresponding to different levels of design abstraction behavioral structural and physical The behavioral level describes the functionality of the design It consists of two components static and dynamic The static component describes

operations whereas the dynamic component describes sequencing and timing The structural level contains information about components control and connectivity The physical level describes the constraints that should be imposed on the floor plan the placement of components and the geometry of the design Constraints of area speed and power are also applied at this level To implement such multilevel transformation a design methodology should be devised taking into consideration the constraints limitations and properties of each level The mapping process between any of these domains is non isomorphic A single behavioral component may be transformed into more than one structural component Design methodologies are the most recent evolution in the design automation era which started off with the introduction and subsequent usage of module generation especially for regular structures such as PLA s and memories A design methodology should offer an integrated design system rather than a set of separate unrelated routines and tools A general outline of a desired integrated design system is as follows Decide on a certain unified framework for all design levels Derive a design method based on this framework Create a design environment to implement this design method

Piecewise Regular Arrays Thomas P Plaks,1999-02-22 Application specific regular array processors have been widely used in signal and image processing multimedia and communication systems for example in data compression and HDTV One of the main problems of application specific computing is how to map algorithms into hardware The major achievement of the theory of regular arrays is that an algorithm represented as a data dependence graph is embedded into a Euclidean space where the integer points are the elementary computations and the dependencies between computations are denoted by vectors between points The process of mapping an algorithm into hardware is reduced to finding for the given Euclidean space a new coordinate system that can be associated with the physical properties of space and time so called space time The power of the synthesis method is that it provides a bridge between abstract and physical representations of algorithms thus providing a methodological basis for synthesizing computations in space and in time This book will extend the existing synthesis theory by exploiting the associativity and commutativity of computations The practical upshot being a controlled increase in the dimensionality of the Euclidean space representing an algorithm This increase delivers more degrees of freedom in the choice of the space time mapping and leads subsequently to more choice in the selection of cost effective application specific designs

Applying Parallel Processing Techniques to Digital Signal Processing Algorithms and Architectures for High Level VLSI Synthesis Lori Ellen Lucke,1992 *A Practitioner's Guide to RISC Microprocessor Architecture* Patrick H. Stakem,1996-04-25 Reduced Instruction Set Computers RISC reduce the number of instructions performed by the microprocessor This volume provides an overview of RISC as both a design philosophy and a marketing and technical force It introduces the fundamentals of RISC mic

Advanced Signal-processing Algorithms, Architectures, and Implementations ,1996 *The Cumulative Book Index* ,1996 A world list of books in the English language **Signal Processing, Theories and Applications** ,1988 **Digital Signal Processing Technology** Society of Photo-optical Instrumentation Engineers,1995 Proceedings of SPIE

present the original research papers presented at SPIE conferences and other high quality conferences in the broad ranging fields of optics and photonics These books provide prompt access to the latest innovations in research and technology in their respective fields Proceedings of SPIE are among the most cited references in patent literature Algorithms and Parallel VLSI Architectures Ed F. Deprettere, Alle-Jan van der Veen, 1991 ARCHITECTURES FOR DIGITAL SIGNAL PROCESSING Peter Pirsch, 2009-08 About The Book This book fuses signal processing algorithms and VLSI circuit design to assist digital signal processing architecture developers The author then shows how this technique can be used in applications such as signal transmission and storage manufacturing process quality control and assurance autonomous mobile system control and biomedical process analysis This new publication is a revised and expanded version Canadian Journal of Electrical and Computer Engineering , 1995 The 1994 IEEE International Conference on Neural Networks , 1994 **ICASSP 88: D, digital signal processing** , 1988 IEEE Workshop on Signal Processing Systems , 1998 High-Performance VLSI Signal Processing Innovative Architectures and Algorithms, Algorithms and Architectures K. J. Ray Liu, Kung Yao, 1998 Electrical Engineering Signal Processing High Performance VLSI Signal Processing Innovative Architectures and Algorithms Volume 1 Algorithms and Architectures The first volume in a two volume set High Performance VLSI Signal Processing Innovative Architectures and Algorithms brings together the most innovative papers in the field focused introductory material and extensive references The editors present timely coverage of algorithm and design methodologies with an emphasis on today s rapidly evolving high speed architectures for VLSI implementations These volumes will serve as vital resources for engineers who want a comprehensive knowledge of the extremely interdisciplinary field of high performance VLSI processing The editors provide a practical understanding of the merits of total system design through an insightful synergistic presentation of methodology architecture and infrastructure Each volume features Major papers that span the wide range of research areas in the field Chapter introductions including historical perspectives Numerous applications oriented design examples Coverage of current and future technological trends Thorough treatment of high speed architectures **VLSI Systems for DSP and Control** Roger Woods, J. V. McCanny, John McCanny, George Irwin, 1991 **CASES 2004** Mary Jane Irwin, 2004

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