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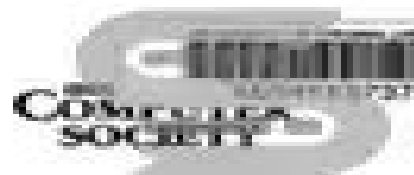
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2006 IEEE International Workshop on Memory Technology, Design, and Testing ,2006 **Advanced Test Methods for SRAMs** Alberto Bosio,Luigi Dilillo,Patrick Girard,Serge Pravossoudovitch,Arnaud Virazel,2009-10-08 Modern electronics depend on nanoscaled technologies that present new challenges in terms of testing and diagnostics Memories are particularly prone to defects since they exploit the technology limits to get the highest density This book is an invaluable guide to the testing and diagnostics of the latest generation of SRAM one of the most widely applied types of memory Classical methods for testing memory are designed to handle the so called static faults but these test solutions are not sufficient for faults that are emerging in the latest Very Deep Sub Micron VDSM technologies These new fault models referred to as dynamic faults are not covered by classical test solutions and require the dedicated test sequences presented in this book **Dissertatiuncula physica de frigore proximi mensis Januarii insolito ... exposita per G.E. Krafft** ,1709 **Memory Technology, Design and Testing: Proceedings, 7th IEEE International Workshop, San Jose, California, 1999** R Rajsuman,1999 **Proceedings International Workshop on Memory Technology, Design and Testing** ,1998 **Multi-run Memory Tests for Pattern Sensitive Faults** Ireneusz Mrozek,2018-07-06 This book describes efficient techniques for production testing as well as for periodic maintenance testing specifically in terms of multi cell faults in modern semiconductor memory The author discusses background selection and address reordering algorithms in multi run transparent march testing processes Formal methods for multi run test generation and many solutions to increase their efficiency are described in detail All methods presented ideas are verified by both analytical investigations and numerical simulations Provides the first book related exclusively to the problem of multi cell fault detection by multi run tests in memory testing process Presents practical algorithms for design and implementation of efficient multi run tests Demonstrates methods verified by analytical and experimental investigations *Records of the IEEE International Workshop on Memory Technology, Design and Testing* David Lepejian,1998 Annotation The 14 papers in this collection from

the August 2001 workshop are divided into five sessions on semiconductor memory design BIST redundancy and error control fault models and multi port SRAM testing and verification and testing Some of the topics are evaluation of redundancy analysis algorithms a parallel approach for testing multi port static random access memories a low output resistance charge pump for flash memory programming BIST based bitfail mapping of an embedded DRAM and an orthogonal transpose RAM cell array architecture with an alternate bit line to bit line contact scheme No subject index c

Book News Inc **Models in Hardware Testing** Hans-Joachim Wunderlich,2009-11-12 Model based testing is the most powerful technique for testing hardware and software systems Models in Hardware Testing describes the use of models at all the levels of hardware testing The relevant fault models for nanoscaled CMOS technology are introduced and their implications on fault simulation automatic test pattern generation fault diagnosis memory testing and power aware testing are discussed Models and the corresponding algorithms are considered with respect to the most recent state of the art and they are put into a historical context by a concluding chapter on the use of physical fault models in fault tolerance 2001 IEEE International Workshop on Memory Technology, Design and Testing ,2001 Proceedings ,2005 Proceedings of the IEEE International Workshop on Memory Technology, Design and Testing , IEEE VLSI Test Symposium ,2004
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