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Network Processor Design

Issues and Practices
Volume 2

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Network Processor Design Vol 2 Issues And Practices:

 Network Processor Design Mark A. Franklin,Patrick Crowley,Haldun Hadimioglu,Peter Z. Onufryk,2005-03-11 The past few years have seen significant change in the landscape of high end network processing In response to the formidable challenges facing this emerging field the editors of this series set out to survey the latest research and practices in the design programming and use of network processors Through chapters on hardware software performance and modeling Network Processor Design illustrates the potential for new NP applications helping to lay a theoretical foundation for the architecture evaluation and programming of networking processors Like Volume 2 of the series Volume 3 further shifts the focus from achieving higher levels of packet processing performance to addressing other critical factors such as ease of programming application developments power and performance prediction In addition Volume 3 emphasizes forward looking leading edge research in the areas of architecture tools and techniques and applications such as high speed intrusion detection and prevention system design and the implementation of new interconnect standards Investigates current applications of network processor technology at Intel Infineon Technologies and NetModule Presents current research in network processor design in three distinct areas Architecture at Washington University St Louis Oregon Health and Science University University of Georgia and North Carolina State University Tools and Techniques at University of Texas Austin Academy of Sciences China University of Paderborn Germany and University of Massachusetts Amherst Applications at University of California Berkeley Universidad Complutense de Madrid Spain ETH Zurich Switzerland Georgia Institute of Technology Vrije Universiteit the Netherlands and Universiteit Leiden the Netherlands   **Network Processor Design** Mark A. Franklin,Patrick Crowley,Haldun Hadimioglu,Peter Z. Onufryk,2002-10-16 As the demand for digital communication networks has increased so have the challenges in network component design To meet ever escalating performance flexibility and economy requirements the networking industry has opted to build products around network processors These new chips range from task specific processors such as classification and encryption engines to more general purpose packet or communications processors Programmable yet application specific their designs are tailored to efficiently implement communications applications such as routing protocol analysis voice and data convergence firewalls VPNs and QoS Network processor design is an emerging field with issues and opportunities both numerous and formidable To help meet this challenge the editors of this volume created the first Workshop on Network Processors a forum for scientists and engineers from academia and industry to discuss their latest research in the architecture design programming and use of these devices In addition to including the results of the Workshop in this volume the editors also present specially commissioned material from practicing designers who discuss their companies latest network processors Network Processor Design Issues and Practices is an essential reference on network processors for graduate students researchers and practicing designers Includes contributions from major academic and industrial research labs including Aachen University of Technology Cisco Systems Infineon

Technologies Intel Corp North Carolina State University Swiss Federal Institute of Technology University of California Berkeley University of Dortmund University of Washington and Washington University Examines the latest network processors from Agere Systems Cisco IBM Intel Motorola Sierra Inc and TranSwitch   *Network Processor Design* ,2004   *Building ASIPs: The Mescal Methodology* Matthias Gries,Kurt Keutzer,2006-07-01 An increasing number of system designers are using ASIP s rather than ASIC s to implement their system solutions Building ASIPs The Mescal Methodology gives a simple but comprehensive methodology for the design of these application specific instruction processors ASIPs The key elements of this methodology are Judiciously using benchmarking Inclusively identifying the architectural space Efficiently describing and evaluating the ASIPs Comprehensively exploring the design space Successfully deploying the ASIP This book includes demonstrations of applications of the methodologies using the Tipi research framework as well as state of the art commercial toolsets from CoWare and Tensilica   *The IEEE Computer Society's 12th Annual International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunications Systems (MASCOTS 2004)* ,2004 MASCOTS 2004 looks at how models can be calibrated and validated against real world observations The papers explore wireless and mobile networks networks and protocols stochastic models queueing networks Internet architecture and applications P2P systems routing algorithms and storage systems   **Euro-Par 2013: Parallel Processing Workshops** Dieter an Mey,Michael Alexander,Bientinesi Paolo,Mario Cannataro,Carsten Clauss,Alexandru Costan,Gabor Kecskemeti,Christine Morin,Laura Ricci,Julio Sahuquillo,Martin Schulz,Vittorio Scarano,Scott Ostercamp,Josef Weidendorfer,2014-04-10 This book constitutes thoroughly refereed post conference proceedings of the workshops of the 19th International Conference on Parallel Computing Euro Par 2013 held in Aachen Germany in August 2013 The 99 papers presented were carefully reviewed and selected from 145 submissions The papers include seven workshops that have been co located with Euro Par in the previous years Big Data Cloud Second Workshop on Big Data Management in Clouds Hetero Par 11th Workshop on Algorithms Models and Tools for Parallel Computing on Heterogeneous Platforms HiBB Fourth Workshop on High Performance Bioinformatics and Biomedicine OMHI Second Workshop on On chip Memory Hierarchies and Interconnects PROPER Sixth Workshop on Productivity and Performance Resilience Sixth Workshop on Resiliency in High Performance Computing with Clusters Clouds and Grids UCHPC Sixth Workshop on Un Conventional High Performance Computing as well as six newcomers DIHC First Workshop on Dependability and Interoperability in Heterogeneous Clouds Fed ICI First Workshop on Federative and Interoperable Cloud Infrastructures LSDVE First Workshop on Large Scale Distributed Virtual Environments on Clouds and P2P MHPC Workshop on Middleware for HPC and Big Data Systems PADABS First Workshop on Parallel and Distributed Agent Based Simulations ROME First Workshop on Runtime and Operating Systems for the Many core Era All these workshops focus on promotion and advancement of all aspects of parallel and distributed computing   Processor Efficiency for Packet-processing Applications Elizabeth Seamans,2005

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